

### INTERVIEW SUMMARY

On 27 June 2003, the undersigned engaged in a telephonic interview with the Examiner regarding the status of the claims. In the telephonic interview, the undersigned related that he had made a typographical error in one of the amended claims (herein corrected), but that the recitations in the Remarks section of the previous Response did not contain that typographical error. The undersigned and the Examiner also discussed the previous response, and the Examiner suggested ways in which the Applicants could clarify their intent. At the conclusion of the interview, the Examiner suggested that Applicants file the present Amendment After Final to clarify previously made points and to correct the typographical error.

Also during the interview, the undersigned pointed out that this Amendment After Final was in no way meant to be argumentative, but rather clarifying. The Examiner noted that it would be taken that way.

### REMARKS

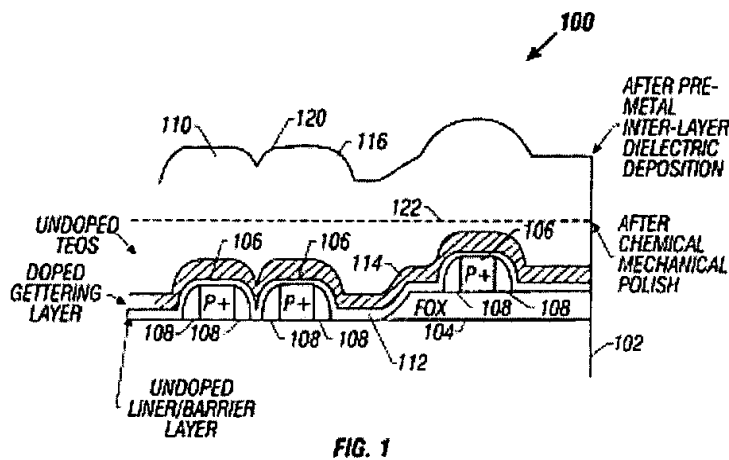
#### STATUS OF CLAIMS

Claims 1-4, 6, 7, 9, 10, 20 and 22-28 are pending in the application. Claims 1-4, 20, and 22-27 stand allowed. *Examiner's Final Office Action* p. 3 (22 May 2003). Claims 6, 7, 9, 10, and 28 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Figures 1-3 of Ngo et al. (U.S. 6,127,261) in view of Figure 7b Dawson (U.S. 5,503,882). *Examiner's Final Office Action* pp. 2-3 (22 May 2003).

#### DISCUSSION

As noted above, the Examiner has rejected Claims 6, 7, 9, 10, and 28 under 35 U.S.C. 103(a) as being unpatentable over Figures 1-3 of Ngo et al. (U.S. 6,127,261) in view of Figure 7b Dawson (U.S. 5,503,882). Figure 1 of Ngo and Figure 7b of Dawson are reproduced following.

FIG. 1 of Ngo is as follows:



With respect to FIG. 1, the text of Ngo states as follows:

Referring to FIG. 1, a cross-sectional view of an integrated circuit 100 shows an example of a trilayer premetal interlayer dielectric deposition. The integrated circuit 100 includes a silicon substrate 102. A field oxide region 104 is formed on one side of the substrate 102 and is used to isolate devices within the substrate 102. A plurality of polysilicon gates 106 are formed overlying the substrate 102. The polysilicon gates 106 have oxide spacers 108 for implantation of structures such as lightly-doped drain (LDD) structures. A tri-layer premetal dielectric 110 overlies the surface of the substrate 102. The three layers of the tri-layer premetal dielectric 110 include an undoped liner/barrier layer 112, a doped gettering layer 114 and an undoped TEOS layer 116. A solid line 120 shows the surface of the integrated circuit 100 overlying the tri-layer premetal dielectric 110 after deposition of the tri-layer but before any etching or polishing. A **dotted line 122 shows the surface of the integrated circuit 100 overlying the tri-layer premetal dielectric 110 after chemical mechanical polishing.**

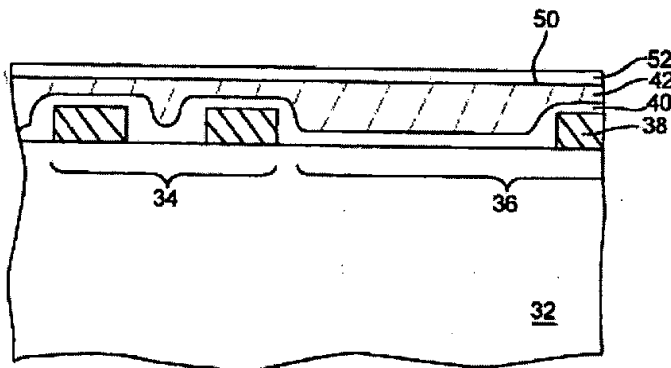
*Ngo Patent*, col. 2, lines 31-49.

The undoped TEOS layer 116 is utilized to fill any voids in the surface of the doped gettering layer 114. **The undoped TEOS layer 116 fills voids caused by structures such as the polysilicon gates 106 and the field oxide region 104. The undoped TEOS layer 116 also adds thickness to the surface of the integrated circuit so that all structures, even prominent structures overlying both the field oxide region 104 and the polysilicon gate 106 [are covered].** The undoped TEOS layer 116 has a thickness of approximately 10200 angstroms. The total thickness of the trilayer premetal dielectric 110 is approximately 13700 angstroms with a standard deviation of approximately 200 angstroms and a final thickness after polishing of about 4000 angstroms.

*Ngo Patent*, col. 2, lines 65-68 and col. 3, lines 1-10 (the sentence stated above is missing the verb and applicants have placed the words “are covered” at the end because it is believed this is what was intended by the inventor and corresponds to what is shown in the figure).

As noted, Ngo teaches that its **“undoped TEOS layer 116 ... adds thickness to the surface of the integrated circuit so that all structures, even prominent structures overlying both the field oxide region 104 and the polysilicon gate 106 [are covered].”** From the specification teachings regarding the structure of Ngo, looking at Figure 1 of Ngo two teachings of Ngo are clear. First, Ngo stops the etch of the TEOS layer 116 well before exposing the upper gettering layer 114. Namely, the dotted line 122 in Figure 1 is well above the upper surface of the doped gettering layer 114 such that the doped gettering layer is not exposed. Second, Ngo teaches that the thickness of the overall structure is increased. Ngo specifically states that the layer 116 is made sufficiently thick that even after the polishing, it is sufficiently thick that all prominent structures including the regions over the field oxides and the polysilicon are completely covered. This second teaching also indicates that it is desired to add to the thickness of the structure as a whole.

Figure 7b of U.S. Patent No. 5,503,882 to Dawson is instructive and is reproduced as follows:



**Fig. 7b**

With respect to FIG. 7b, the text of Dawson states as follows:

Alternatively, capping layer 52 can be placed upon an etch-back upper surface 50 of FIG. 6b, as shown in FIG. 7b. Capping layer 52, in either embodiments of FIG. 7a or 7b, provide the advantages described above. Capping layer 52 upon etch-back upper surface 50, shown in FIG. 7b, ensures that the lower density TEOS oxide will not absorb moisture from an outside ambient. Capping layer 52

provides a barrier against absorption similar to the barrier formed above SOG layer 46, as shown in FIG. 7a.

*Dawson Patent*, col. 9 lines 21-30

Applicants believe that the present amendment to **Claim 6** corrects the typographical error that led the Examiner to reject Claim 6. Specifically Applicants have herein amended claim 6 to recite **“an unplanar layer of borophosphorous silicate glass disposed on the layer of undoped silicate glass, said unplanar layer having an uppermost surface; a planar dielectric layer disposed on the unplanar layer of borophosphorous silicate glass, said planar dielectric layer having an uppermost surface substantially even with the uppermost surface of said unplanar layer of borophosphorous silicate glass; and a second dielectric layer disposed on the planar dielectric layer and the uppermost surface of said unplanar layer of borophosphorous silicate glass, said layer of undoped silicate glass, said layer of borophosphorous silicate glass, said planar dielectric layer, and said second dielectric layer together composing a pre-metal dielectric stack.”** As can be seen from Ngo’s Fig. 1 and supporting text, Ngo does not show at least the foregoing highlighted recitations of herein amended claim 6. As can be seen in Fig. 7b of Dawson, layer 52 resides on top of another PETEOS layer 42. Accordingly, even if Ngo and Dawson were combined, they would still fail to teach at least the **“an unplanar layer of borophosphorous silicate glass disposed on the layer of undoped silicate glass, said unplanar layer having an uppermost surface; a planar dielectric layer disposed on the unplanar layer of borophosphorous silicate glass, said planar dielectric layer having an uppermost surface substantially even with the uppermost surface of said unplanar layer of borophosphorous silicate glass; and a second dielectric layer disposed on the planar dielectric layer and the uppermost surface of said unplanar layer of borophosphorous silicate glass, said layer of undoped silicate glass, said layer of borophosphorous silicate glass, said planar dielectric layer, and said second dielectric layer together composing a pre-metal dielectric stack”** recitations of herein amended Claim 6. Accordingly, the art of record does not render herein amended Claim 6 unpatentable. Consequently, Applicants respectfully ask that the Examiner hold Claim 6 allowable over the art of record for at least the foregoing reasons.

Claims 7, 9, and 10 depend from Claim 6, and are hence allowable for at least the reasons of such dependencies.

Claim 28 recites **“a layer of borophosphorous silicate glass over the layer of undoped silicate glass, said layer of borophosphorous silicate glass having an upper surface having a highest surface region and a lowest surface region; a planarized layer of plasma-enhanced tetraethyl orthosilicate disposed on said layer of borophosphorous silicate glass said planarized layer having a thickness less than or approximately equal to a difference in the highest surface region and the lowest surface region of the BPSG layer; and a layer of plasma-enhanced tetraethyl orthosilicate overlaying and being in contact with the planarized layer of plasma-enhanced tetraethyl orthosilicate and directly overlaying and being in contact with the highest surface region of the borophosphorous silicate glass region....”** As can be seen from Ngo’s Fig. 1 and supporting text, Ngo does not show at least the foregoing highlighted recitations of herein amended claim 28. Accordingly, the art of record does not render Claim 28 unpatentable. Consequently, Applicants respectfully ask that the Examiner hold Claim 28 allowable over the art of record for at least the foregoing reasons.

Patentability now established, the remainder of the rejections are rendered moot, and hence Applicants do not explicitly address such moot rejections herein. The fact that the moot rejections are not addressed should not be taken as an admission of any sort, and Applicants reserve the right to contest the statements in such moot rejections at a later time, should such become necessary.

The Commissioner is authorized to charge any additional fees due by way of this Amendment, or credit any overpayment, to our Deposit Account No. 19-1090.

All of the claims remaining in the application are now clearly allowable. Favorable consideration and a Notice of Allowance are earnestly solicited.

Respectfully submitted,

Shin Hwa Li et al.

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